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Code No. : 13208 O

VASAVI COLLEGE OF ENGINEERING (Autonomous), HYDERABAD
B.E. (CSE) II Year I-Semester Backlog Examinations, December-2017

Computer Architecture

Time: 3 hours

Max. Marks: 70

Note: Answer ALL questions in Part-A and any FIVE from Part-B

Part-A (10 × 2 = 20 Marks)

1. How would you convert decimal value 41.6875 into binary?
2. Consider a memory unit that receives the address from address register, AR. The data from memory transferred to data register, DR. Write symbolic notations for Read and Write operations.
3. Perform the following operations on the given binary numbers A = 1010 and B = 1101 using
 - i) Selective Complement
 - ii) Selective Clear.
4. How would you determine memory reference instruction type is direct or indirect for the binary instruction 1010 0000 1111 0000?
5. From the information given, the pipeline has 4 segments and executes 100 tasks each segment will take 20 ns. How many ns will take to complete the task?
6. Write a symbolic micro-program for the fetch routine.
7. Distinguish between vectored interrupt and non- vectored interrupt.
8. What is the use of software routines in priority interrupt?
9. How the performance of cache memory is measured?
10. Why virtual memory is superior to auxiliary memory?

Part-B (5 × 10 = 50 Marks)

11. a) Design basic computer components of a system? Explain with bus structure. [4]
b) What is (r-1)'s complement? Find out the 9's complement of 546700? [6]
12. a) What is a program interrupt? Design a flow chart for interrupt cycle? [4]
b) A computer uses a memory unit with 256M words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has three parts: an indirect bit, an operation code, and an address part. [6]
 - i) How many bits are there in the operation code?
 - ii) How many bits are there in the address part?
13. a) Explain different types of instruction formats used in basic computers. [5]
b) Evaluate (-9) * (-6) using booth's multiplication algorithm. [5]
14. a) Explain input-output processor with neat block diagram. [4]
b) A CPU with a 20-MHz clock is connected to a memory unit whose access time is 40 ns. Formulate a read and write timing diagrams using a READ strobe and a WRITE strobe. Include the address in the timing diagram. [6]

15. a) Explain segmented page mapping with the help of suitable example. [4]
 b) A digital computer has a memory unit of $64K \times 16$ and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words. [6]
 i) How many bits are there in the tag, index, block and word fields of the address format?
 ii) How many bits are there in each word of the cache, and how are they divided into functions? Include the valid bit.
 iii) How many blocks can the cache accommodate?
16. a) Explain floating point representation with an example. [4]
 b) For decimal number +70, perform the following operations and write the equivalent decimal number. (Consider an 8 bit register) [6]
 i) Circular shift right
 ii) Arithmetic shift right
 iii) Can we perform arithmetic shift left on +70? Justify.
17. Answer any *two* of the following:
 a) Design and explain the micro-program sequencer. [5]
 b) What is the importance of DMA? [5]
 c) Explain about set associative mapping. [5]

